Using FPGAs for Spectrum Sensing and Modulation Recognition Project

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Date: 07/09/2020

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Project Overview

- Project seeks to use machine learning to recognize different wireless devices
- Use software defined radios (SDRs) to record various devices as training data for neural nets
- Classify type of device based on RF signature

Last Week

- Research and learn about how to implement and use matched filters, specifically RRC (root-raised cosine) matched filter
- Run OEDL script on grid, finished debugging

The Experiment

Goal: Mimic WiFi transmissions in a (mostly) controlled environment and be able to classify each transmission based on its modulation scheme.

Hardware: USRP X310, USRP B210

Software: MATLAB, UHD, OEDL

Target Modulations: BPSK, QPSK, 16QAM, 64QAM

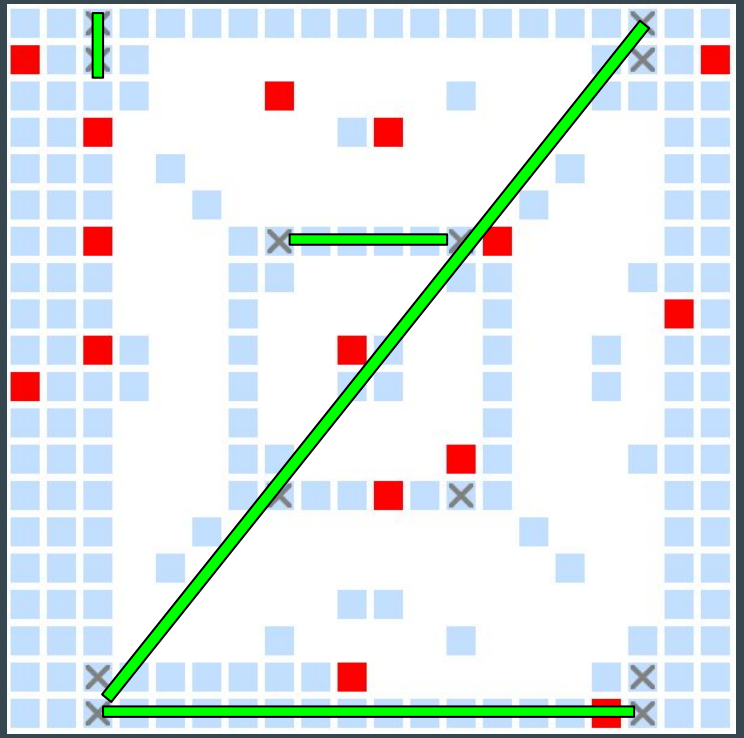
The Experiment

Constants

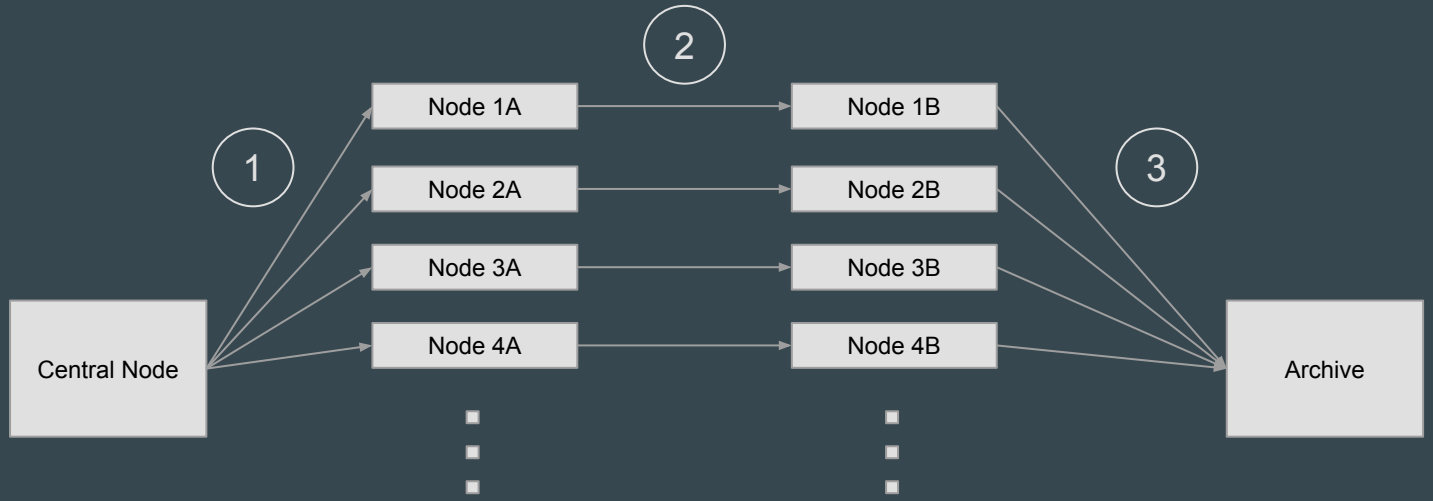
Transmitter Bandwidth	20 Mhz
Receiver Sampling Rate	40 MSps
Input/Output Binary File Format	Float32
Packet Payload Size	1500 Bytes

Variables

Gain	TBD
Distance (ft)	3, 15, 45, 72
Frequency (Mhz)	2412, 2437, 2462, 5180, 5240, 5745, 5825
Modulation and Coding Scheme (MCS)	0, 1, 2, 3, 4, 5, 6, 7



Experiment Flow



1. Copy WiFi IQ sample files to set “A” nodes (transmitters)
2. Transmit WiFi IQ sample files via USRP to set “B” nodes (receivers)
3. Copy received WiFi IQ sample files to archival storage

* Each A-B node pair represents a topology defined by the physical distance between the nodes

Matched Filter

- What it is:
  - Take a “template” signal and compare it to an unknown signal
  - Determine if the template is present in the unknown signal
  - If the template is present, we know the modulation scheme of the unknown signal
- What it is to us:
  - NN Based Modulation Recognition
    - Requires very little a priori information
    - Used for signals we know very little about
  - Matched Filter
    - Requires a priori information (cannot work without it)
    - Used for signals we have decent knowledge of
  - Performance Comparison

Plans for next week

- Begin implementing a simple RRC matched filter using MATLAB to get the idea
- Later, create a matched filter in Go to be used in the argo2verilog compiler to generate Verilog code to used for FPGA implementation
- Continue collection data on Grid
- Work more on the website

Questions?